ABSTRACT OF THE DISCLOSURE

The present invention provides a processor capable of carrying out a plurality of operation instructions simultaneously in one cycle which improves utilization of an instruction when carrying out a single operation instruction, and a system equipped with such a processor. In this processor, an operation mode indicating whether or not a coprocessor should be run in parallel is retained in an operation mode register, and in the integer processor operation mode, a value "0" is set in the operation mode register in an operation mode controller of an integer processor, and an instruction register delivers an integer processor instruction to a decoder, so that an execution unit will execute the integer processor instruction, and outputs a no operation instruction to a data processor without embedding an instruction that defines an operation thereof, and puts the data processor in the halt condition. On the other hand, in the parallel processing operation mode, a value "1" is set in the operation mode register in the operation mode controller, and the instruction register delivers the integer processor instruction to the decoder, and outputs a data processor instruction to the data processor to carry out data processing. Because the integer processor operation mode requires the integer processor instruction alone in the instruction string, utilization of the instructions can be improved.